CLAIMS

1. A semiconductor device having a read only storage device which outputs data read from a memory cell in response to storage device selection information and address information, and a switching device wherein

said switching device comprises:

an address storage circuit for storing said address information of a defective memory cell of said read only storage device;

a data storage circuit for storing the replacement data of said defective memory cell; and

a switching circuit which inputs the output data from said read only storage device and the output data from said data storage circuit, and outputs either of said two pieces of output data based on said address information stored in said address storage circuit.

2. A semiconductor device having a plurality of read only storage devices which share an output data line and output data read from a memory cell in response to storage device selection information and address information, and a switching device wherein

said switching device comprises:

an address storage circuit for storing said storage device selection information and said address information of a defective memory cell of at least one of said read only storage devices;

a data storage circuit for storing the replacement data of said defective memory cell; and

a switching circuit which inputs the output data output from said read only storage device via said output data line and the output data from said data storage circuit, and outputs either of said two pieces of output data based on said storage device selection information and said address information stored in said address storage circuit.

3. A semiconductor device having a plurality of read only storage devices, each of which includes a separate output data line and outputs data read from a memory cell in response to storage device selection information and address information, and a switching device wherein

said switching device comprises:

an address storage circuit for storing said storage device selection information and said address information of a defective memory cell of at least one of said read only storage devices;

a data storage circuit for storing the

replacement data of said defective memory cell; and

a plurality of switching circuits individually placed at each said output data line, which input the output data output from said read only storage device via said output data line and the output data from said data storage circuit, and output either of said two pieces of output data based on said storage device selection information and said address information stored in said address storage circuit.

4. A semiconductor device in accordance with any of claims 1 to 3, wherein

instead of said data storage circuit, a bit storage circuit for storing bit information of a defective bit of said defective memory cell, or said bit storage circuit for storing bit information of a defective bit and a data storage circuit for storing the replacement data of said defective bit are provided, and

said switching circuit inputs the output data from said read only storage device, and an inversed signal of the output data from said read only storage device or the output data from said data storage circuit or fixed data of 0 or 1, selects either of them based further on said bit information and outputs the selection by the bit.

5. A semiconductor device having a rewritable storage device which is provided with redundancy memory cells and outputs data read from its memory cell array in response to storage device selection information and address information, a read only storage device which outputs data read from its memory cell array in response to said storage device selection information and said address information, and a switching device wherein

said switching device comprises:

an address storage circuit for storing said storage device selection information and said address information of a defective memory cell of said rewritable storage device, and said storage device selection information and said address information of a defective memory cell of said read only storage device;

a data storage circuit for storing the replacement data of said defective memory cell of said read only storage device; and

a switching circuit which inputs the output data from said read only storage device and the output data from said data storage circuit, and outputs either of said two pieces of output data based on said storage device selection information and said address

information stored in said address storage circuit, and

said rewritable storage device outputs either the output data read from the usual memory cell array or the output data read from said redundancy memory cell based on said storage device selection information and said address information stored in said address storage circuit.